CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An image array pixel comprising:

   a charge sharing node; and

   a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node.

2. The pixel of claim 1, wherein said first voltage is higher than said second voltage.

3. The pixel of claim 2, wherein said second voltage is a ground potential.

4. The pixel of claim 1, wherein said one of said source/drain regions is coupled to only one of said first and second voltages at a time.

5. The pixel of claim 1, wherein said pixel does not receive any light.

6. The pixel of claim 1, wherein said pixel is a three-transistor pixel.

7. The pixel of claim 1, wherein said pixel is a four-transistor pixel.

8. A pixel circuit, comprising:

   a photo sensor;

   a storage node for receiving charges from said photo sensor; and

   a reset transistor for resetting said storage node, said reset transistor being switchably coupled to a first and second voltage level.

9. The pixel of claim 8, wherein said first voltage level is lower than said second voltage level.

10. The pixel of claim 8, wherein said second voltage level is a ground potential

11. The pixel of claim 8, wherein said pixel is a three-transistor pixel.

12. The pixel of claim 8, wherein said pixel is a four-transistor pixel.

13. An image array pixel comprising:

a change storing node;

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node; and

a source-follower transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions of said source-follower transistor being coupled to said first and second voltage and to said one of said source/drain regions of said reset transistor.

14. The pixel of claim 13, wherein said first voltage is higher than said second voltage.

15. The pixel of claim 13, wherein said second voltage is a ground potential.

16. The pixel of claim 13, wherein said first source/drain of reset transistor is coupled only to one of said first and second voltages at a time.

17. The pixel of claim 13, wherein said pixel is does not receive any light.

18. An image array comprising:

a pixel cell;

a power supply circuit for selectively providing a first and second reset voltage; and

a switch circuit for coupling said power supply circuit to a storage node of said pixel cell.

19. The image array of claim 18, wherein said power supply circuit comprises:

a first transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first voltage, the other of said source/drain regions being coupled to said storage node; and

a second transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a second voltage, the other of said source/drain regions being coupled to said storage node.

20. The image array of claim 19, wherein said only one of said first and second transistors of said power supply circuit is conductive at the same time.

21. The image array of claim 20, wherein said first voltage is substantially equal to an operating voltage of a pixel array.

22. The image array of claim 20, wherein said second voltage is a lower voltage than said first voltage.

23. The image array of claim 22, wherein said second voltage is a ground potential.

24. The image array of claim 19, wherein said switch circuit comprises:

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to said output of said power supply circuit, the other of said source/drain regions being coupled to said storage a node.

25. The image array of claim 24, further comprising:

a reset control circuit for controlling said reset transistor in said pixel cell, said reset control circuit coupled to said gate of said reset transistor.

26. The image array of claim 25, wherein said reset control circuit provides a first and second reset control signal.

27. The image array of claim 26, wherein said first control signal is a full reset control signal.

28. The image array of claim 27, wherein said second control signal is an intermediate reset control signal.

29. The image array of claim 19, wherein first pixel cell is a light opaque pixel cell.

30. The image array of claim 19, wherein first pixel cell is disposed in a redundant area of said array.

31. The image array of claim 25, wherein said power supply circuit is mutually coupled to a second pixel cell.

32. The image array of claim 31, wherein second pixel cell is disposed in a same row of said image array as said first pixel cell.

33. A method of operating pixel of pixel array, said method comprising:

flooding a pixel in said array to clear any stored signal;

applying a first reset voltage to said charge storage area of said pixel;

sampling a first voltage signal from said charge storage area;

applying a second reset voltage to said charge storage area;

sampling a second voltage signal from said charge storage area; and

determining a difference between said first and second sampled voltage signals.

34. The method of claim 33, wherein said first reset voltage is an intermediate reset voltage, which is less than a full reset voltage.

35. The method of claim 34, wherein said second reset voltage said full reset voltage.

36. The method of claim 33, wherein said first reset voltage is a higher voltage than said second reset voltage.

37. The method of claim 36, wherein said determining further comprises:

determining said difference in a differential amplifier.

38. The method of claim 37, further comprising:

converting said difference into a digital form.

39. A method of determining the intermediate reset voltage of an image array, said method comprising:

sampling and storing a first set of integrated signals from an array of pixels;

applying a first reset voltage to said array of pixels;

sampling and storing a first set of reset signals from said array of pixels;

applying a second reset voltage to said array of pixels;

sampling and storing a second set of integrated signals from said array of pixels;

applying said first reset voltage to said array of pixels;

sampling and storing a second set of reset signals from said array of pixels; and

determining a difference between said first set and second set of sampled voltage signals.

40. The method of claim 39, wherein said first reset voltage is a full reset voltage.

41. The method of claim 40, wherein said second reset voltage is an intermediate reset voltage.

42. The method of claim 39, wherein said first reset voltage is a higher voltage than said second reset voltage.

43. The method of claim 39, wherein said determining step comprises:

determining a difference between said first set of integrated and reset sampled and stored voltage signals in a differential amplifier to provide a set of difference signals.

44. The method of claim 43, wherein said determining step further comprises:

determining a difference between said second set of integrated and reset sampled and stored voltage signals in a differential amplifier to provide a second set of difference signals.

45. The method of claim 44, wherein said determining step further comprises:

converting said first set of difference signals into a set of digital values.

46. The method of claim 45, wherein said determining step further comprises:

converting said second set of difference signals into a second set of digital values.

47. The method of claim 46, wherein said determining step further comprises:

comparing said first and second sets of digital values.

48. The method of claim 47, wherein said comparing step comprises:

offsetting said first set of digital values by said second set of digital values.

49. The method of claim 46, wherein said determining step further comprises:

identifying saturated pixels from said first set of digital values.

50. The method of claim 49, further comprising:

offsetting said first set of digital values corresponding to said saturated pixels by said second set of digital values corresponding to said saturated pixels.

51. The method of claim 50, wherein said applying said second reset voltage occurs shortly before said sampling and storing said second set of integrated signals.

52. A processing system, comprising:

a processor;

an imager array coupled to said processor, one pixel of said image array comprising:

a charge sharing node; and

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node.

53. The processing system of claim 52, wherein said first voltage is higher than said second voltage.

54. The processing system of claim 53, wherein said second voltage is a ground potential.

55. The processing system of claim 52, wherein said one of said source/drain regions is coupled to only one of said first and second voltages at a time.

56. A processor system, comprising:

a processor;

an imager array coupled to said processor, one pixel of said imager array comprising:

a pixel cell;

a power supply circuit for reflectively providing a first and second reset voltage; and

a switch circuit for coupling said power supply circuit to a storage node of said pixel cell.

57. The processor system of claim 56, wherein said power supply circuit further comprises:

a first transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first voltage, the other of said source/drain regions being coupled to said storage node; and

a second transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a second voltage, the other of said source/drain regions being coupled to said storage node.

58. The processor system of claim 57, wherein said only one of said first and second transistors of said power supply circuit is conductive at the same time.

59. The processor system of claim 58, wherein said first voltage is substantially equal to an operating voltage of a pixel array.

60. The processor system of claim 58, wherein said second voltage is a lower voltage than said first voltage.

61. The processor system of claim 60, wherein said second voltage is a ground potential.

62. The processor system of claim 57, wherein said switching circuit comprises:

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to said output of said power supply circuit, the other of said source/drain regions being coupled to said storage node.

63. The processor system of claim 62, further comprising:

a reset control circuit for controlling said reset transistor in said pixel cell, said reset control circuit coupled to said gate of said reset transistor.

64. The processor system of claim 63, wherein said reset control circuit provides a first and second reset control signal.

65. The processor system of claim 64, wherein said first control signal is a full reset control signal.

66. The processor system of claim 58, wherein said second control signal is an intermediate reset control signal.

67. An imaging device, comprising:

a processor;

an imager array coupled to said processor, one pixel of said image array comprising:

a charge sharing node; and

a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node.

68. The imaging device of claim 67, wherein said first voltage is higher than said second voltage.

69. The imaging device of claim 68, wherein said second voltage is a ground potential.

70. The imaging device of claim 67, wherein said one of said source/drain regions is coupled to only one of said first and second voltages at a time.